Paper Code(s): ECC-207	**L**	**P**	**C**
Paper: Digital Logic and Computer Design	**4**	**-**	**4**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1^{st}) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To introduce basic concepts of Boolean Algebra and Combinational Logic
2.	To introduce various sequential circuits, designing with examples
3.	To relate combination circuit design and sequential circuit design with respect to the design of a computer system
4.	To introduce machine learning, computer arithmetic, modes of data transfer with respect to I/O and Memory organization of a computer

Course Outcomes (CO) :

CO 1	Ability to understand Boolean Algebra and Design Combinational Circuits .
CO 2	Ability to understand and Design Sequential Circuits.
CO 3	Ability to understand Design of a basic computer.
CO 4	Ability to understand Input-Output and Memory Organization of a Computer.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	2	3	2	2	-	-	-	3	2	2	3
CO 2	3	2	3	2	2	-	-	-	3	2	2	3
CO 3	3	2	3	3	2	-	-	-	3	2	2	3
CO 4	3	3	3	3	3	-	-	-	3	2	2	3

UNIT – I

Boolean Algebra and Combinational Logic: Review of number systems , signed, unsigned, fixed point, floating point numbers, Binary Codes, Boolean algebra – basic postulates, theorems , Simplification of Boolean function using Karnaugh map and Quine-McCluskey method – Implementations of combinational logic functions using gates, Adders, Subtractors, Magnitude comparator, encoder and decoders, multiplexers, code converters , parity generator/checker, implementation of combinational circuits using multiplexers.

UNIT – II

Sequential Circuits: General model of sequential circuits, Flip-flops, latches , level triggering, edge triggering, master slave configuration , concept of state diagram , state table, state reduction procedures , Design of synchronous sequential circuits , up/down and modulus counters , shift registers, Ring counter , Johnson counter , timing diagram , serial adder , sequence detector, Programmable Logic Array (PLA), Programmable Array Logic (PAL), Memory Unit, Random Access Memory

UNIT – III

Basic Computer organization: Stored Program, Organization, Computer registers, bus system, instruction set completeness, instruction cycle, Register Transfer Language, Arithmetic, Logic and Shift Micro-operations, Instruction Codes, Design of a simple computer, Design of Arithmetic Logic unit, shifter, Design of a simple hardwired control unit, Programming the basic computer, Machine language instructions, assembly language, Microprogrammed control, Horizontal and Vertical Microprogramming, Central Processing Unit, instruction sets and formats, addressing modes, data paths, RISC and CISC characteristics.

UNIT – IV

Computer Arithmetic, addition, subtraction, multiplication and division algorithms, Input-Output Organization, Modes of data transfer, Interrupt cycle, direct memory access, Input-Output processor, Memory Organization, Memory Hierarchy, Associative Memory, Cache Memory, Internal and external Memory, Virtual Memory.

Text Book(s)

1. M. Morris Mano, "Digital Logic and Computer Design", Pearson Education, 2016
2. M. Morris Mano, Rajib Mall "Computer System Architecture", 3rd Edition Pearson Education, 2017

References:

1. Leach, D. P., Albert P. Malvino, "Digital Principles and Applications", McGraw Hill Education, 8th Edition , 2014
2. Jain, R.P. ,"Modern Digital Electronics", McGraw Hill Education, 4th Edition , 2010
3. Floyd, Thomas L. , "Digital Fundamentals" Pearson Education, 11th Edition, 2017
4. M. Rafiquzzaman, "Fundamentals of Digital Logic and Microcomputer Design", Wiley, 5th Ed., 2005.